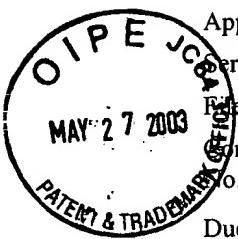


05-29-03

9P2123

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicant: HEGDE ET AL. Examiner: H. DAY
Serial No.: 09/495,150 Group Art Unit: 2123
Filed: JANUARY 31, 2000 Docket: 30019.103US01
Confirmation No.: 4464
Due Date: MAY 24, 2003
Title: METHOD AND APPARATUS FOR HARDWARE AND SOFTWARE CO-SIMULATION

CERTIFICATE UNDER 37 CFR 1.10:

"Express Mail" mailing label number: EV347850215US
Date of Deposit: May 27, 2003

I hereby certify that this paper or fee is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Mail Stop NON-FEE AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By: *Joshua N. Randall*
Name: Joshua N. Randall

Mail Stop NON-FEE AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RECEIVED

MAY 30 2003

Sir:

Technology Center 2100

We are transmitting herewith the attached:

- Transmittal Sheet in duplicate containing Certificate of Mailing
- Amendment and Response Including Version With Markings To Show Changes Made
- Return postcard

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers or any future reply, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

MERCHANT & GOULD P.C.
P.O. Box 2903, Minneapolis, MN 55402-0903
612.332.5300

By: *Joshua N. Randall*
Name: Joshua N. Randall
Reg. No.: 50,719
JRandall:PSTdb





PATENT

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Applicant: HEGDE ET AL. Examiner: H. DAY
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By: Junkers
Name: John Junkers

AMENDMENT AND RESPONSE

RECEIVED

MAY 30 2003

Technology Center 2100

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed on February 24, 2003, please enter the following amendments and remarks.

In the Claims

Please cancel claim 13.

Please amend claims 1, 2, 8, 12 and 14 as follows:

1. (Amended) A method of developing an ASIC using a hardware model, a software, and a network, the hardware model comprising a CPU bus functional model, the software being coupled to a CPU server, and the network configured to provide communication between the hardware model and the software, the method comprising the steps of: